Amendments to the Claims:

The following claims will replace all prior versions of the claims in this application (in the unlikely event that no claims follow herein, the previously pending claims will remain):

1. (Currently Amended) A microcontroller, comprising:

a clock input pin, wherein an input signal from ~~the~~ an external circuit is inputted;

a clock generating means for generating a clock signal by receiving a signal from the clock input pin;

a clock output pin for receiving the clock signal of the clock generating means and outputting the clock signal in a clock generation mode;

a first switch, enabled in a predetermined system mode, for transmitting an internal signal of the microcontroller to the clock output pin for using the clock output pin ~~in a predetermined system mode~~; and

a second switch, which is coupled between the clock generating means and the clock output pin, enabled in the clock generation mode for transmitting the clock signal between the clock generating means and the clock output pin and disabled in the predetermined system mode.

2. (Previously Presented) The microcontroller as recited in claim 1, wherein the second switch includes a plurality of switches connected in parallel.

3. (Previously Presented) The microcontroller as recited in claim 2, further comprising a control means for selectively controlling each of switches depending on a clock signal of the clock input pin.

4. (Previously Presented) The microcontroller as recited in claim 1, further comprising a control means for selectively enabling first and second switches classified by modes.

5. (Previously Presented) The microcontroller as recited in claim 2, further comprising a control means for selectively controlling each of switches depending on a clock signal of the clock input pin and selectively enabling first and second switches classified by modes.

6. (Previously Presented) The microcontroller as recited in claim 1, wherein the clock generating means includes: an inverter for amplifying an input signal as a full-swing to generate a clock signal; and a resistor, which is connected to input and output terminals of the inverter.

7. (Currently Amended) A system having a microcontroller, comprising:

a clock input pin for receiving an input signal;

a first clock generating means for receiving a signal from the clock input pin to generate a clock signal;

a first switch for transmitting an internal signal of the microcontroller to the clock output pin for using ~~a~~ the clock output pin in a predetermined system mode;

a second switch, which is coupled between the clock generating means and the clock output pin, enabled in the clock generation mode for transmitting the clock signal between the clock generating means and the clock output pin and disabled in the predetermined system mode; and

a second clock generating means for providing a clock signal to the microcontroller through the clock input pin in the predetermined system mode.

8. (Previously Presented) The system as recited in claim 7, wherein the second switch includes a plurality of switches connected in parallel.

9. (Previously Presented) The system as recited in claim 8, further comprising a control means, which is placed in either inside or outside of the microcontroller, for selectively controlling each of switches depending on a frequency of a clock signal of the clock input pin.

10. (Previously Presented) The system as recited in claim 7, further comprising a control means, which is placed in either inside or outside of the microcontroller, for selectively controlling each of switches depending on a clock signal of the clock input pin and selectively enabling first and second switches classified by modes.

11. (Previously Presented) The system as recited in claim 8, further comprising a control means, which is placed in either inside or outside of the microcontroller, for selectively controlling each of switches depending on the frequency of the clock signal of the clock input pin and for selectively controlling each of switches depending on a clock signal of the clock input pin and selectively enabling first and second switches classified by modes.